

## PC/104

### 6 Channel Single Speed or Two-Speed, Programmable

Encoder & Velocity Outputs, 16-Bit; Continuous Self Test;  
Equivalent Hall Effect (A, B, C) Commutation Outputs (Optional)  
Cumulative Turns Register (Optional)  
On-Board Programmable Reference Supply (Optional)  
16 Programmable TTL Digital I/O

### FEATURES

- Only +5 VDC
- 16 bit resolution (up to 24 bit for two-speed mode)
- $\pm 1$  arc minute accuracy for single speed.
- Continuous background BIT testing
- **Self-calibrating (Does not require removal)**
- Either single or two speed configurable (channel pairs)
- Encoder (A & B) plus Index outputs; Programmable
- Equivalent Hall Effect (A,B,C) commutation outputs
- Synchro / Resolver Programmable option
- Bandwidth of each channel is programmable
- Cumulative Turns counter option
- 47 Hz to 10 KHz
- Digital Velocity outputs
- Latch feature
- Synthetic reference compensates for  $\pm 60^\circ$  phase shift
- Two banks of 8 (16 total) digital I/O. Input/output (programmable for each bank)
- No adjustments or trimming required



### DESCRIPTION:

This DSP based compliant stack-through module offers six (6) separate isolated Synchro/Resolver-to-Digital tracking converters, 16 TTL Digital I/O, extensive diagnostics, digital velocity outputs and optional Reference and turn counters. Each channel also produces differential incremental encoder (A&B) outputs (with programmable resolution) and a zero degree marker pulse. Commutation outputs are available for 4, 6, or 8 pole brushless DC motors that eliminate the need for Hall Effect sensors on the motor thus eliminating processor time and reducing bus traffic. Any combination of two-speed and single-speed channels can be field programmed to any ratio between 1 and 255. Ambiguity circuits maintain monotonic outputs by compensating for misalignment between the Coarse and Fine Synchros; however, the processor will set a flag when it senses that the maximum allowable misalignment of  $90^\circ/\text{gear ratio}$  is exceeded. This card, even when large accelerations are encountered, never loses tracking, because it incorporates the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 rps, at 16-bit resolution. The "Latch" feature permits user to read all channels at the same time. Reading will unlatch that channel. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that current valid data is always available for any channel without affecting the tracking performance of the converters. A watchdog timer is provided to monitor the processor. Resolver inputs are auto-ranging that eliminates the need to specify input voltages in advance. Part #, S/N, Date code, & Rev. are stored in non-volatile memory.

A Windows® based software support kit (SSK) including drivers and sample soft-panel application is available.

## **DIAGNOSTICS AND BUILT-IN-TEST (BIT):**

**This board incorporates major diagnostics** that offer substantial improvements to system reliability because user is alerted to channel malfunction. This approach reduces bus traffic because the Status registers need not be constantly polled. Three different tests (one on-line and two off-line) can be selected:

**The (D2) test** initiates automatic background BIT testing (on-line). Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. The results are available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

**The (D3) test** initiates a BIT test that disconnects all channels (off-line) from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05° (off-line). Results can be read from registers. External reference is not required. Testing requires no external programming, and can be initiated or stopped via the bus.

**The (D0) test** is used to check the card and the PC-bus interface (off-line). All channels are disconnected from the outside world, allowing user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

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## SPECIFICATIONS

### Synchro / Digital

Resolution:	16 bits
Accuracy:	±1 arc minute for single speed inputs 1 arc minute divided by gear ratio for two-speed inputs
Tracking Rate:	150 rps max. Referred to Fine input in a two-speed configuration
Bandwidth:	Default is 40Hz for 400Hz carrier version and 100 Hz above 1 KHz carrier version. Can be readily programmed.
Input format:	Synchro or Resolver, (programmable)
Gear ratio:	Each channel pair is programmable from 2 to 255
Input voltage:	Resolver / Synchro 2-28 V <sub>L-L</sub> Auto-ranging or 90 V <sub>L-L</sub> Galvanic isolation
Input Impedance:	40 kΩ min. up to 28 V <sub>L-L</sub> , 100 kΩ min. at 90 V <sub>L-L</sub>
Reference:	2-115 Vrms, Auto-ranging. Galvanic isolation.
Reference Zin	100 kΩ min.
Frequency:	47 Hz to 10 KHz (See part number).
Encoder outputs:	Either 12,13,14,15, or 16 bit resolution, (field programmable) and Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N).
Commutation outputs:	Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16 bit resolution; Linearity: 0.1%. Scaleable to 0.1°/sec resolution.
Power:	+ 5 VDC @ 1.25 A (1.75 A peak) (Add additional 1A @ 3VA Load with optional Reference Supply)
Temperature, operating:	-40°C to +85°C;
Storage temperature:	-55°C to +105°C.
Conformal Coating:	Both sides of the board can be conformal coated (See part number).
Weight:	4 oz.

### Reference Supply

Voltage:	Optional (See part number configurator) 2-28 Vrms, programmable, resolution 0.1 Vrms. Or 115 Vrms fixed. Galvanic isolation.
Accuracy	± 3%
Distortion:	± 2% THD
Frequency:	360 Hz to 10 KHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	3 VA max. @ 40° min. inductive; 115 mA max @ 26 VAC; 26 mA @ 115 VAC Note: Power (VA) is reduced linearly as the Reference Voltage decreases.
Ground:	Isolated from system ground

### Digital I/O

TTL and CMOS compatible. Includes bus hold. Therefore, when used as inputs, no external pull-up or pull-down resistors are required.

V<sub>out L</sub>: 0.55 V max. at I<sub>OL</sub> of 64 mA max.

V<sub>out H</sub>: 2.0 V min. at I<sub>OH</sub> of 32 mA max.

V<sub>out H</sub>: 3.0 V min. at I<sub>OH</sub> of 3 mA

V<sub>in L</sub>: 0.8 V

V<sub>in H</sub>: 2.0 V

V<sub>in max</sub>: 5.0 V

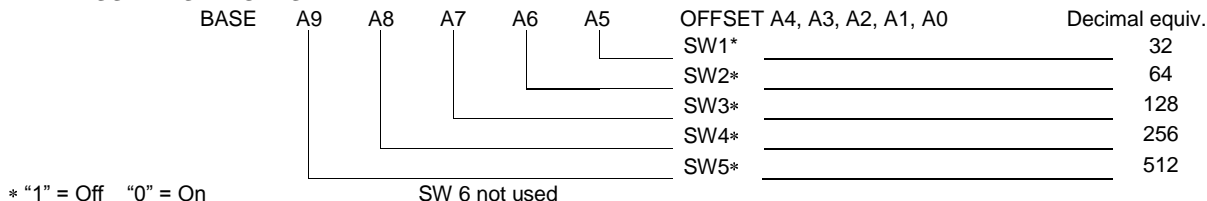
## PROGRAMMING INSTRUCTIONS

This card offers many options. Any option that is not required may be ignored. Channels are referred to from 1 to 6. For two-speed applications, channel pairs are generally referred as the Coarse and Fine inputs. For example, two-speed channel pair 1 and 2: Channel 1 would be considered Coarse, channel 2 becomes Fine. Channel pair 3 and 4: channel 3 becomes Coarse, channel 4 becomes fine, etc.

### I/O Configuration

This card requires 32 consecutive addresses in the I/O address space on a 32 byte boundary. The base address is switch settable in the 000-3E0 hex (0 to 392) address range.

**ADDRESS= BASE + OFFSET**



**NOTE: Base addresses to avoid:**

378-37F	Parallel Printer Port	3B0-3BF	Monochrome Display	3F8-3FF	Asynch Comm I/O	3F0-3F7	Floppy Disk
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### Register Bit Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data (°) Hi <sup>1</sup>	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data (°) Lo <sup>1</sup>	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
Latch outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Active channels	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
TTL Digital I/O	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Bank Select	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D0
Status, Reference	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Signal	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Angle Δ Change Alert	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Summary	X	X	X	X	X	X	X	X	X	X	#6	#5	#4	#3	#2	#1
Two-speed lock loss	X	X	X	X	X	X	X	X	X	X	Ch.5/6	X	Ch.3/4	X	Ch.1/2	X
(A & B) resolution:	D15	X	X	X	X	X	X	X	X	X	X	X	X	D2	D1	D0

↑ : "0" = Encoder

"1" = Commutation

(A & B) resolution: ↓

Note 1 – values are rounded off.

4 pole	16 bit	0	0	0
6 pole	15 bit	0	0	1
8 pole	14 bit	0	1	0
Commutation outputs ↑	13 bit	0	1	1
	12 bit	1	0	0

Synchro / RSL Select	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00 = Resolver format	X	X	X	X	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1						
11 = Synchro format																

### SUMMARY STATUS REGISTER

#1 = S/D Signal Loss

#2 = S/D Reference Loss

#3 = S/D Angle Change Alert (Global – Read Angle Change Alert Register for particular channel failure)

#4 = S/D Test Accuracy Error

## Page Specific Register Map

### Page 1 (1E = 0)

00	Ch.1 Data Hi	R	08	Ch.5 Data Hi	R	10	Ch.2 Data Lo	R	18	Ratio Ch. 2/1	W/R
02	Ch.2 Data Hi	R	0A	Ch 6 Data Hi	R	12	Ch.4 Data Lo	R	1A	Ratio Ch. 4/3	W/R
04	Ch.3 Data Hi	R	0C	Not used		14	Ch.6 Data Lo	R	1C	Ratio Ch. 6/5	W/R
06	Ch.4 Data Hi	R	0E	Not used		16	Two-speed Lock Loss	R	1E	Page Register = 0	W/R

### Page 2 (1E = 1)

00	Ch.1 Velocity	R	08	Ch.5 Velocity	R	10	Ch.1 Velocity Scale	W/R	18	Ch.5 Velocity Scale	W/R
02	Ch.2 Velocity	R	0A	Ch.6 Velocity	R	12	Ch.2 Velocity Scale	W/R	1A	Ch.6 Velocity Scale	W/R
04	Ch.3 Velocity	R	0C	Not used		14	Ch.3 Velocity Scale	W/R	1C	Not used	
06	Ch.4 Velocity	R	0E	Not used		16	Ch.4 Velocity Scale	W/R	1E	Page Register = 1	W/R

### Page 3 (1E = 2)

00	Active channels	W/R	08	Latch	W	10	Status, Signal Loss	R	18	Not Used	
02	Test D2 verify	W/R	0A	Not Used		12	Status, Reference Loss	R	1A	Osc Frequency	W/R
04	Test Enable	W/R	0C	Board Ready	R	14	Status, Test	R	1C	Osc Voltage	W/R
06	Test Angle	W/R	0E	Not used		16	Status, Summary	R	1E	Page Register = 2	W/R

### Page 4 (1E = 3)

00	Ch.1 Angle $\Delta$	W/R	08	Ch.5 Angle $\Delta$	W/R	10	Ch.1 (A & B) resolution	W/R	18	Ch.5 (A & B) resolution	W/R
02	Ch.2 Angle $\Delta$	W/R	0A	Ch.6 Angle $\Delta$	W/R	12	Ch.2 (A & B) resolution	W/R	1A	Ch.6 (A & B) resolution	W/R
04	Ch.3 Angle $\Delta$	W/R	0C	Angle $\Delta$ Initiate	W/R	14	Ch.3 (A & B) resolution	W/R	1C	Not used	
06	Ch.4 Angle $\Delta$	W/R	0E	Angle $\Delta$ Change Alert	W/R	16	Ch.4 (A & B) resolution	W/R	1E	Page Register = 3	W/R

### Page 5 (1E = 4)

00	Watchdog timer	W/R	08	Date Code	R	10	Not Used		18	Not used	
02	Soft reset	W	0A	PCB rev.	R	12	Not used		1A	Not used	
04	Part Number	R	0C	DSP rev.	R	14	Not used		1C	Not used	
06	Serial Number	R	0E	FPGA rev.	R	16	Not used		1E	Page Register = 4	W/R

### Page 6 (1E = 5)

00	0-7 Bank select	W/R	08	Not used		10	Not used		18	Not used	
02	8-15 Bank select	W/R	0A	Not used		12	Not used		1A	Not used	
04	Output	W/R	0C	Not used		14	Not used		1C	Not used	
06	Input	W/R	0E	Not used		16	Not used		1E	Page Register = 5	W/R

### Page 7 (1E = 6)

00	Ch.1 Cumulative Turns	W/R	08	Ch.5 Cumulative Turns	W/R	10	Not used		18	Not used	
02	Ch.2 Cumulative Turns	W/R	0A	Ch.6 Cumulative Turns	W/R	12	Not used		1A	Not used	
04	Ch.3 Cumulative Turns	W/R	0C	Not used		14	Not used		1C	Not used	
06	Ch.4 Cumulative Turns	W/R	0E	Not used		16	Not used		1E	Page Register = 6	W/R

### Page 8 (1E = 7)

00	Ch.1 Bandwidth	W/R	08	Ch.5 Bandwidth	W/R	10	Not used		18	Not used	
02	Ch.2 Bandwidth	W/R	0A	Ch.6 Bandwidth	W/R	12	Not used		1A	Not used	
04	Ch.3 Bandwidth	W/R	0C	Bandwidth Select	W/R	14	Not used		1C	Not used	
06	Ch.4 Bandwidth	W/R	0E	Not used		16	Not used		1E	Page Register = 7	W/R

### Page 9 (1E = 8)

00	SYN / RSL SEL	W/R	08	Not used		10	Backwards compatibility mode, status logic	W/R	18	Not used	
02	Not used		0A	Not used		12	Not used		1A	Not used	
04	Not used		0C	Not used		14	Not used		1C	Not used	
06	Not used		0E	Not used		16	Not used		1E	Page Register = 8	W/R

### Page 10 (1E = 9)

00	Ch.1 S/D Freq Lo	R	08	Ch.3 S/D Freq Lo	R	10	Ch.5 S/D Freq Lo	R	18	Not used
02	Ch.1 S/D Freq Hi	R	0A	Ch.3 S/D Freq Hi	R	12	Ch.5 S/D Freq Hi	R	1A	Not used
04	Ch.2 S/D Freq Lo	R	0C	Ch.4 S/D Freq Lo	R	14	Ch.6 S/D Freq Lo	R	1C	Not used
06	Ch.2 S/D Freq Hi	R	0E	Ch.4 S/D Freq Hi	R	16	Ch.6 S/D Freq Hi	R	1E	Page Register = 9 W/R

### Page 11 (1E = A)

00	Ch.1 S/D VLL	R	08	Ch.5 S/D VLL	R	10	Ch.3 VREF	R	18	Not used
02	Ch.2 S/D VLL	R	0A	Ch.6 S/D VLL	R	12	Ch.4 VREF	R	1A	Not used
04	Ch.3 S/D VLL	R	0C	Ch.1 VREF	R	14	Ch.5 VREF	R	1C	Not used
06	Ch.4 S/D VLL	R	0E	Ch.2 VREF	R	16	Ch.6 VREF	R	1E	Page Register = A W/R

### Page 12 (1E = B)

00	Ch.1 S/D VLL Loss Threshold W/R	08	Ch.5 S/D VLL Loss Threshold W/R	10	Ch.3 S/D RefV Loss Threshold W/R	18	Not used
02	Ch.2 S/D VLL Loss Threshold W/R	0A	Ch.6 S/D VLL Loss Threshold W/R	12	Ch.4 S/D RefV Loss Threshold W/R	1A	Not used
04	Ch.3 S/D VLL Loss Threshold W/R	0C	Ch.1 S/D RefV Loss Threshold W/R	14	Ch.5 S/D RefV Loss Threshold W/R	1C	Not used
06	Ch.4 S/D VLL Loss Threshold W/R	0E	Ch.2 S/D RefV Loss Threshold W/R	16	Ch.6 S/D RefV Loss Threshold W/R	1E	Page Register = B W/R

### Page 13 (1E = C)

00	S/D SIG STAT INT ENBL W/R	08	S/D Angle Chg INT ENBL W/R	10	Not Used	18	Not used
02	S/D REF STAT INT ENBL W/R	0A	Not Used	12	Not Used	1A	Not used
04	S/D BIT STAT INT ENBL W/R	0C	Not Used	14	Not Used	1C	Not used
06	S/D Lock STAT INT ENBL W/R	0E	Not Used	16	Not Used	1E	Page Register = C W/R

### Page 14 (1E = D) (Factory Use Only – “htext”)

00		08		10		18	
02		0A		12		1A	
04		0C		14		1C	
06		0E		16		1E	

### Page 15 (1E = E) (Factory Use Only – “htext”)

00		08		10		18	
02		0A		12		1A	
04		0C		14		1C	
06		0E		16		1E	

### Page 16 (1E = F) (Factory Use Only – “htext”)

00		08		10		18	
02		0A		12		1A	
04		0C		14		1C	
06		0E		16		1E	



## S/D FUNCTIONS

### Power On Reset or System Reset

All parameters are restored to initial defaults. A power on automatic calibration test is run and completes in approximately 30 seconds.

### Active Channels

Set the bit corresponding to each channel to be monitored during BIT testing in the *S/D Active Channel Register* ("1"=active; "0"=not used). **Omitting this step will produce errors on unused channels causing false alarms;** hence unused channels will set faults, i.e. status bits, interrupts, etc.

### Ratio

Applies to 2-speed measurement; Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

### Read

For single speed applications (Ratio=1), read individual channels 1, 2, 3, 4, etc. For two-speed applications, read only channels (2, 4, 6, 8, etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word. In 2-speed applications, the COMBINED 2-speed angle measurement result is available from the even channel register of the channel pair.

### Two-Speed Connectivity Instructions

In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4, CH5 & 6.

### Two-Speed Lock Loss

The card monitors misalignment between Coarse and Fine angles during two-speed operation. A two-speed lock loss condition exists if the maximum allowable misalignment between the Coarse and Fine angles of 90°/ratio is exceeded. The corresponding bit for that channel pair in the *Two-Speed Lock-Loss Register* will be set to "1" for "Lock Loss".

### Latch

The Angle and the Cumulative turns (optional) for all channels can be obtained by writing "1" to D1 of Latch register. Reading a particular channel will disengage the latch for that channel. Writing a '0' to the D1 bit of the latch register will unlatch all channels.

### Velocity Output

Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

- When max. velocity is set to 152.5878 rps, an actual speed of 10 rps CW would be read as 0863h.
- When max. velocity is set to 152.5878 rps, an actual speed of 10 rps CCW would be read as F79Ch.
- When max. velocity is set to 50.8626 rps, an actual speed of 10 rps CW would be read as 192Ah.
- When max. velocity is set to 50.8626 rps, an actual speed of 10 rps CCW would be read as E6D5h.

To convert a velocity word to rps: **Velocity in rps = Maximum x Output / Full Scale**

Example: If Velocity Output were E6D5h, and maximum velocity were 50.8626 rps, then

$$\text{Velocity in rps} = 50.8626 \times \text{E6D5h} / 32,768 = 50.8626 \times -6,442 / 32,768 = -10 \text{ rps}$$



## Velocity Scale Factor

The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (rps). The scale factor is: **4095(152.5878rps/max rps)**, where the max rps is selected by the user to achieve the maximum resolution for a desired rps. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

- To scale the Max Velocity word for 152.5878 rps, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 rps for CW rotation, and -32,768 (8000h) being 152.5878 rps for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.
- To get a max vel word (32,767) @ 152.5878 rps, Scale Factor =  $4095(152.5878/152.5878) = 4095 = 0FFFh$ ; This results in a velocity resolution of:  $(152.5878 \text{ rps}/32,767) \times 360^\circ/\text{rps} = 1.676^\circ/\text{sec}$  (factory default)
- To get a max vel word (32,767) @ 50.8626 rps, Scale Factor =  $4095(152.5878/50.8626) = 12,285 = 2FFDh$ ; This is a velocity resolution of:  $(50.8626 \text{ rps}/32,767) \times 360^\circ/\text{rps} = 0.5588^\circ/\text{sec}$
- For 9.5367 rps max, Scale Factor =  $4095(152.5878/9.5367) = 65,520 = FFF0h$ ;  $0.10477^\circ/\text{sec}$  resolution

## Bandwidth

The bandwidth for each channel is individually programmable when the *Bandwidth Select* register channel is set to "Manual". The minimum BW is 2 Hz, and the maximum BW is 1000 Hz. LSB is 1 Hz. Write desired BW as unsigned integer, between 2 and 1000, to associated channel register. All values greater than 1000 will be processed as 1000 Hz. All values less than 2 will be processed as 2 Hz. When *Bandwidth Select* register channel is set to "Automatic", *Bandwidth* register will report the channel bandwidth.

When in "Manual BW" mode, the user can enter the BW between a range of 2 Hz and 1000 Hz, in 2 Hz increments.

## Bandwidth Select

BW Select register sets the "Automatic" or "Manual" Bandwidth control. This register is bitmapped per channel; (i.e. D0 = CH1, D1 = CH2, etc.). "1" indicates automatic bandwidth. "0" indicates manual control.

The Automatic BW feature, when enabled, reads the input reference frequency and automatically adjusts the BW to approximately 1/10 of the carrier frequency. This Auto BW range will be a minimum of 6 Hz with a maximum of 1280 Hz.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	FUNCTION
BANDWIDTH SELECT	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D=DATA BIT

## Synchro / Resolver Selection

Each measurement channel can be programmed for either synchro or resolver input signal format. Writing a "0" to both D1 and D0 of the *Synchro / Resolver Selection* register sets channel 1 to resolver format. Writing a "1" to D1 and D0 of the *Synchro / Resolver Selection* register sets channel 1 to synchro format (follow corresponding bit pattern for other channels).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Synchro/Resolver Format Select	X	X	X	X	X	X	X	X	X	X	CH3		CH2		CH1	

## Input Reference Frequency Measurement

Each individual channel input reference frequency is measured and the value reported to a corresponding read register. The input reference frequency is reported to a resolution of 0.01 Hz. The output is in integer decimal format. For example, if channel 1 input reference is 400 Hz, the output measurement word from the corresponding register would be 40,000.

## Input Signal Voltage (V<sub>L-L</sub>) Measurement

Each individual channel input signal voltage "V<sub>L-L</sub>" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180.

## Input Reference Loss Detection Threshold

Each individual channel input reference voltage is measured. By setting the Input Reference Loss detection threshold, the user has capability of tailoring when reference loss detection is indicated during the D2 background test. The reference loss threshold is set by entering the voltage level in decimal integer format to a resolution of 10 mv. For example, if the user wishes channel 1 reference loss threshold set for 2 Vrms, the register would be set to 200.

## Input Signal Loss Detection Threshold

Each individual channel input signal voltage is measured. By setting the Input Signal Loss detection threshold, the user has capability of tailoring when signal loss detection is indicated during the D2 background test. The signal loss threshold is set by entering the voltage level in decimal integer format to a resolution of 10 mv. For example, if the user wishes channel 1 signal loss threshold set for 4 Vrms, the register would be set to 400.

## D2 Test Enable

Writing "1" to the D2 bit of the *Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. The result of an accuracy error is available in the *Test Status Register*. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. The card will write 55h to the *Test (D2) Verify Register*, every 0.1 seconds, when the D2 Test is enabled. User can periodically clear the *Test (D2) Verify Register* by writing 00h, waiting 0.1 seconds, then reading the register again to verify that background BIT testing is activated.

In addition, each Signal and Reference is continually monitored. The results are available in the *Signal* and *Reference Status Registers*.

## Angle Change Alert

Write a 16-bit word to the appropriate *Angle Change Register* for a given channel, to represent the minimum differential change required. MSB=180°; Minimum differential is 0.05°, setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring by writing "1" to *Angle Change Initiate Register*.

When that differential is exceeded, on any monitored channel, the bit corresponding to that channel is set in *Angle Change Alert Register* ("0" = no change, "1" = change).

## D3 Test Enable

Writing "1" to the D3 bit of the *Test Enable Register* initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. The test cycle is completed within 45 seconds and results can be read from the *Test Status Registers* when D3 bit changes from "1" to "0". The testing can be terminated at any time by writing "0" to D3 bit of the *Test Enable Register*.

Signal and Reference monitoring is disabled during D3 test.

## D0 Test Enable

Used to check card and PC interface. Writing "1" to the D0 bit of the *S/D Test Enable Register* disconnects all channels from the outside world, enabling the user to generate any test angle by writing an integer value, to the *Test Angle Register*. Data is then read through the interface (after writing, allow 400 ms before reading). External reference is not required. (e.g. 330° = angle/(360/2<sup>16</sup>)).

Signal and Reference monitoring is disabled during D0 test.

## Status, Test (Fail)

Check the channel's corresponding bit of the *Test Status Register* for status (accuracy BIT) for each active channel. A "0" means accuracy passes; A "1" indicates a failure on an active channel. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register.

## Status, Reference (Loss)

Check the channel's corresponding bit of the *Reference Status Register* for status of the reference input for each active channel. A "1" means Reference LOSS, a "0" means Reference valid or "OK" (as compared with value set in *Reference Loss Detection Threshold* register) on active channels. Channels that are inactive are also set to "0". (Reference loss is detected within 2 seconds). Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

This register also corresponds with the *Input Reference Loss Detection Threshold Register*.

## Status, Signal (Loss)

Check the corresponding bit of the *Signal Status Register* for status of the input signals for each active channel. A "1" means Signal "LOSS" (level compared with value set in *Signal Loss Threshold* register), a "0" means Signal valid or "OK" on active channels. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Any signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms, registers will be updated with the background data. Allow 250 ms to scan all channels.

This register also corresponds with the *Input Signal Loss Detection Threshold Register*.

## Backward Compatibility Mode, Status Logic

The 73SD4 status logic, as defined herein, is reversed as compared to the legacy 73SD1, 73SD2 and 73SD3 models. The *Backward Compatibility Mode, Status Logic* register function provides the ability to query and/or set the logic of the status registers to either default, as defined herein, or reversed to provide "backward compatibility" status logic as defined in the legacy models. Suggested use of this register is for applications requiring legacy status logic. Query and/or set the logic for all status (*Status, Test, Status Reference, Status Signal*). A "0" is default and considered "not" backward compatible logic (status logic matches the descriptions defined herein) and a "1" is backward compatible status logic (status logic is reversed compared to the descriptions defined herein). (functionality introduced @ DOM 03/2014 or greater – master DSP rev. 10 or greater).

## Angle Change Alert

Write a 16-bit word to the appropriate *Angle Change Register* for a given channel, to represent the minimum differential change required. MSB=180°; Minimum differential is 0.05°, setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring by writing "1" to *Angle Change Initiate Register*. When that differential is exceeded, on any monitored channel, the bit corresponding to that channel is set in *Angle Change Alert Register* ("0" = no change, "1" = change).

## Status, Summary

Monitoring a change due to a problem/failure can be accomplished by polling the *Summary Status Register*. By reading the *Summary Status Register*, the user can determine whether a change occurred from Signal Loss, Reference Loss, Angle Change Alert and or Test Accuracy Error. To determine which channel was affected, read the appropriate register. Any status failure, transient or intermittent will latch the *Summary Status Register*. Reading will unlatch register – once register is unlatched, any secondary faults that were captured will propagate – it is recommended to "read until cleared" to allow all previous captured faults to propagate/update clear. (bit mapped; "0" = "pass", "1" = "fault", not affected by *Backward Compatibility Mode, Status Logic* register function).

### Optional (A&B) Encoder Resolution

To set Encoder Mode, write a “0” to the D15 bit and the appropriate code for the desired resolution to the D2, D1 & D0 bits of the corresponding channel to the *(A&B) Resolution/Poles Register*. Changing the resolution for any channel can be done on the fly. The default is a 12bit resolution encoder output.

**Note:** Encoder/Commutation outputs are optional; see part ordering information.

### Optional Commutation Outputs (A, B, C)

To set Commutation Mode, write a “1” to the D15 bit and the appropriate code for the required motor poles to the D2, D1 & D0 bits of the corresponding channel to the *(A&B) Resolution/Poles Register*. See Register Bit map table.

**Note:** Encoder/Commutation outputs are optional; see part ordering information.

### Cumulative Turns (Optional)

The total numbers of turns (complete revolutions), in either direction (CW/CCW) is stored in the *Cumulative Turns Registers* for the corresponding channels and is read as a 2's complement 8-bit integer. To reset the register to zero counts (0000h), write a '0' to the *Cumulative Turns Register*. The register cannot be preloaded. The range is from 7Fh to 80h (2's complement - warning the count will rollover after +/- 127 Turns). CW rotation is positive and CCW rotations are negative. If Turns are to be read in conjunction with Angle Data, it is recommended to use the latch command prior to reading (fractional readings or Turns). Once the latch is issued, the integer is read from the *Cumulative Turns Register* for that particular channel and the corresponding *Data Hi Register* for the fractional portion of the turn. Reading the *Data Hi Register* will unlatch the data for that channel and the *Cumulative Turns Register* for that channel.

### Reference Supply (OSC) (Optional)

For frequency, write a 16-bit word (Ex: 400 Hz = 0x190) to OSC Frequency Register. For voltage, write a word (Ex: 26.1Vrms = 0x105) with LSB = 0.1Vrms, to OSC Voltage Register. It is recommended that user program the required frequency before setting the output voltage.

## DIGITAL I/O FUNCTIONS

### **Bank Select for Digital I/O's**

Controls the direction of each bank of 8, Digital I/O. A "0" in a Bank Select Register sets the corresponding bank to be Inputs. A "1" sets the bank to be Outputs.

### **Input Register**

Indicates the logic state of Digital I/O bits. Upper byte represents bank 8-15, lower byte represents bank 0-7.

### **Output Register**

Controls the logic state of Digital I/O's, when bank is set to be Outputs. Upper-byte controls bank 8-15; lower byte controls bank 0-7.

## ADDITIONAL FUNCTIONS

### **Soft Reset**

Writing a "1" (Level sensitive) to the Soft Reset Register initiates and holds software in reset state. Then, writing "0" initiates reboot (takes 400 ms). Following the soft reset, a power on automatic calibration test is run and completes in approximately 30 seconds. This function is equivalent to Power on Reset.

### **Watchdog Timer**

This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

### **Part Number**

Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

### **Serial Number**

Read as a 16-bit binary word from the *Serial Number Register*. This is the serial number of that particular board.

### **Date Code**

Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week)

### **Rev Levels**

There are a total of 3 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

- Rev level PCB
- Rev level DSP
- Rev level FPGA

## I/O CONNECTORS AND PINOUTS

**JP6:** AMP 104130-9, Mate: AMP 1-746285-0 & strain relief 499252-4

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Ch.3-BHi	9	Ground	17	D I/O 4	25	Ch.1-Ahi	33	Ch.3-S4	41	Ch.2-S1	49	Ch.1-S2
2	Ch.3-BLo	10	Ground	18	D I/O 5	26	Ch.1-Alo	34	Ch.3-S1	42	Ch.2-S3	50	Ch.2-Rhi
3	Ch.3-Alo	11	Ch.3-IDXHi	19	D I/O 6	27	Ch.1-Bhi	35	Ch.3-Rlo	43	Ch.1-S3		
4	Ch.3-Ahi	12	Ch.3-IDXLo	20	D I/O 7	28	Ch.1-Blo	36	Ch.3-Rhi	44	Ch.1-S1		
5	Ch.2-IDXHi	13	D I/O 0	21	Ch.1-IDXHi	29	Ground	37	Rlo-Out	45	Ch.2-S2		
6	Ch.2-IDXLo	14	D I/O 1	22	Ch.1-IDXLo	30	Ground	38	Ch.1-Rlo	46	Ch.2-S4		
7	Ch..2 Blo	15	D I/O 2	23	Ch.2-Ahi	31	Ch.3-S2	39	Rhi-Out	47	Ch.1-S4		
8	Ch..2 Bhi	16	D I/O 3	24	Ch.2-Alo	32	Ch.3-S3	40	Ch.1-Rhi	48	Ch.2-Rlo		

**JP7:** AMP 104130-9, Mate: AMP 1-746285-0 & strain relief 499252-4

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Ch.6-S4	9	Ch.5-S3	17	Ch.4-Rlo	25	Ch.4-IDXHi	33	Ch.6-Ahi	41	D I/O 8	49	Ground
2	Ch.6-Rlo	10	Ch.5-Rhi	18	Ch.4-S4	26	Ch.4-IDXLo	34	Ch.6-Alo	42	D I/O 9	50	Ground
3	Ch.5-S4	11	Ch.6-S1	19	Ground	27	Ch.5-Ahi	35	Ch.6-Bhi	43	D I/O 10		
4	Ch.6-Rhi	12	Ch.4-S3	20	Ground	28	Ch.5-Alo	36	Ch.6-Blo	44	D I/O 11		
5	Ch.5-S2	13	Ch.6-S3	21	Ch.4-Ahi	29	Ch.5-Bhi	37	Ch.6-IDXHi	45	D I/O 12		
6	Ch.6-S2	14	Ch.4-S1	22	Ch.4-Alo	30	Ch.5-Blo	38	Ch.6-IDXLo	46	D I/O 13		
7	Ch.5-S1	15	Ch.4-Rhi	23	Ch.4-Bhi	31	Ch.5-IDXHi	39	Ground	47	D I/O 14		
8	Ch.5-Rlo	16	Ch.4-S2	24	Ch.4-Blo	32	Ch.5-IDXLo	40	Ground	48	D I/O 15		

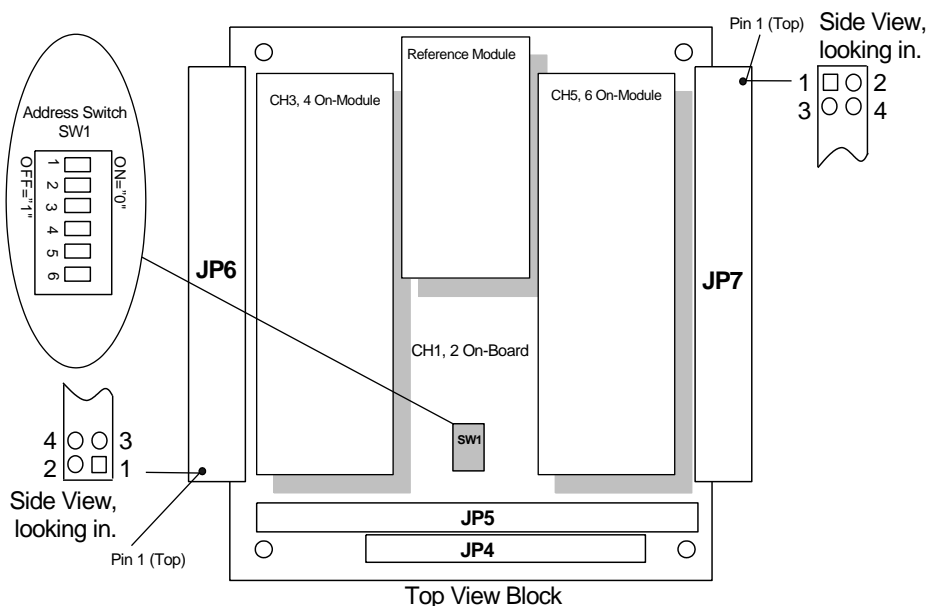
### NOTES:

- Optional Reference output is NOT internally tied to individual channel reference inputs.
- Do not connect to any undesigned pins.
- When commutation outputs (A, B, C) are selected Index+ becomes C+ and Index- becomes C-.
- Pins J5B-10 and J4C-20 have been removed for keying purposes.
- NAI Synchro / Resolver naming convention:

Signal	Resolver	Synchro
S1	SIN(-)	X
S2	COS(+)	Z
S3	SIN(+)	Y
S4	COS(-)	(No connect)

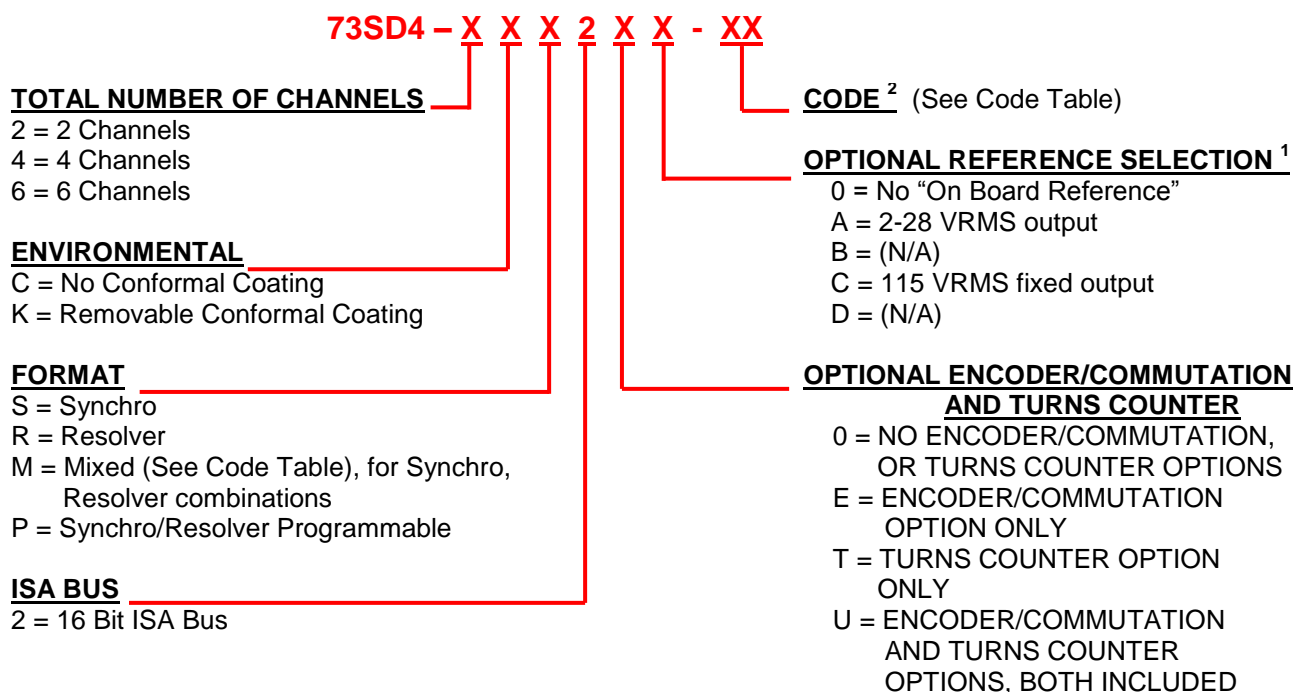
## MECHANICAL

### PC/104, Basic Layout





## PART NUMBER DESIGNATION



### Code Table

Code	Frequency (Hz)	Input (VL-L)	Input (Z)	Ref Vrms	Comments
01	400	11.8	40K	26	
02	400	90	100K	115	
03	50/400	90	100K	115	
04	400	2-26	40K	2-26	
06	2.5 KHz	2-26	40K	2-26	
07	1.2 KHz	2-26	40K	2-26	

### Notes:

1. On-Board Reference **IS** independent output (not connected internally to any S/D channels).
2. Contact Factory for code list addendum for descriptions of code 50 and above.



## REVISION PAGE

Revision	Description of Change	Engineer	Date
1.0	Preliminary Release – Based on 73_SD3_A001_Rev_3.1 / Programming not yet updated with new features.	FH/as	04/18/06
1.2	Added programming extensions (rev 1.1 skipped)	FH/as	05/11/06
1.3	Revised register mapping	AS	02/01/07
1.4	Changed “Discrete” reference to “TTL Digital I/O”; NAI Address update	AS	05/08/07
1.5	Part Number Designation reverts back to “SD3” format	AS	06/01/07
1.6	Clarified REF option specification, 2-28 programmable or 115V fixed (pg. 6)	AS	11/15/07
1.7	Corrected typo – register map pg 12 (VLL to RefV, Ch 3-6)	AS	11/30/07
A	Initial Agile Release	AS	12/03/07
A1	Agile release / minor corrections	AS	12/03/07
A2	Agile re-release / minor corrections	AS	03/25/08
A3	Re-release to Agile / Clarified module slots and address switch layout	AS	03/28/08
A4	Updated Temperature specifications	AS	01/27/10
A5	Added “backward compatibility, status logic” register/function (Page 9 1E=8, register 0)	AS	02/10/14

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